IN THE CLAIMS

Please cancel claims 3-4 and 21 without prejudice.

Please amend claims 1-2, 5-6, 8, 13-14, and 17-20 as indicated below.

1. (Currently Amended) A method comprising:

enabling a special programming mode of a memory by entering a special programming

access code in a state controller, wherein the memory includes automation

circuitry for internal program verification and wherein enabling special

programming mode disables the internal program verification by the

automation circuitry of the memory;

programming a plurality of words into the memory during the special programming

mode without having the automation circuitry of the memory to perform the

internal program verification; ~~and~~

exiting the special programming mode of the memory after the plurality of words have

been programmed into the memory; and

enabling the internal program verification of the memory after exiting the special

programming mode, wherein one or more words subsequently programmed

into the memory are verified by the internal program verification performed by

the memory.

2. (Currently Amended) The method of claim 1, further comprising verifying the plurality of

words programmed into the memory by a verification processor ~~other than~~ externally coupled

to the memory during the special program mode of the memory.

3. – 4. (Canceled)

5. (Currently Amended) The method of claim 2, wherein the verifying further includes:

determining if all of the words in the plurality of words are verified;

if any one of the plurality of words does not verify, then repeating the programming of

the entire plurality of words and repeating the ~~verification~~ verifying by the

verification processor ~~other than the memory~~; and

if all of the plurality of words verify, then exiting the special programming mode of

the memory.

6. (Currently Amended) The method of claim 2, wherein the verifying further includes:

determining if all of the words in the plurality of words are verified;

if any one of the plurality of words does not verify, then repeating the programming of

the word that did not verify and repeating the verification by the verification

processor ~~other than the memory~~; and

if all of the plurality of words verify, then exiting the special programming mode of

the memory.

7. (Previously Presented) The method of claim 1, wherein upon exiting the special

programming mode of the memory, the special programming mode is permanently disabled.

8. (Currently Amended) The method of claim 1, wherein upon exiting the special

programming mode of memory, ~~the~~ internal program verification by the memory is enabled.

9. (Previously Presented) The method of claim 1, wherein the programming of the plurality of words into the memory comprises using only a single programming pulse for each bit of each word of the plurality of words.

10. (Previously presented) The method of claim 1, wherein the programming of the plurality of words into the memory without the memory performing internal program verification continues until a programming ending condition is met.

11. (Original) The method of claim 10, wherein the programming ending condition is a pre-selected time.

12. (Original) The method of claim 10, wherein the programming ending condition is an ending address.

13. (Currently Amended) An apparatus comprising:

a first memory comprising:

an automation circuitry to perform internal program verification unless the automation circuitry is disabled [[;]] , the automation circuitry including

a special programming mode circuitry to disable the automation circuitry that performs the internal program verification when the special programming mode circuitry is enabled; and

a host processor communicatively coupled to the first memory, the host processor

sending to the first memory a first plurality of words to be programmed into the

first memory without the first memory performing the internal program

verification during the special programming mode; ~~and~~

exiting the special programming mode of the first memory after the first

plurality of words have been programmed into the first memory; and

enabling the internal program verification of the first memory after exiting the

special programming mode, wherein one or more words subsequently

programmed into the first memory are verified by the internal program

verification performed by the first memory.

14. (Currently Amended) The apparatus of claim 13, wherein the host processor further

verifies the first plurality of words programmed into the first memory without having the first

memory to perform the internal verification.

15. – 16. (Canceled)

17. (Currently Amended) The apparatus of claim 14, wherein the ~~the~~ host processor, without

invoking the internal program verification performed by ~~of~~ the first memory,

reads back from the first memory the first plurality of words that have been

programmed into the first memory, and

compares ~~the~~ a second plurality of words stored in a second memory coupled to the

host processor with [[a]] the first plurality of words read back from the first

memory to verify whether the first plurality of words have been programmed

into the first memory successfully, the second memory being separated from the first memory and external to the first memory.

18. (Currently Amended) The apparatus of claim 17, wherein the host processor further reprograms the entire first plurality of words into the first memory if any one of the first plurality of words is not verified successfully by the host processor.

19. (Currently Amended) The apparatus of claim 17, wherein the host processor further reprograms one or more of the first plurality of words into the first memory that did not verify successfully without reprogramming a remainder of the first plurality of words that verifies successfully.

20. (Currently Amended) The apparatus of claim 13, wherein the the host processor disables the special programming mode circuitry when exiting the special program mode of the first memory.

21. (Canceled)

22. (Original) The apparatus of claim 13, wherein the special programming mode circuitry is disabled when a programming ending condition is met.

23. (Original) The apparatus of claim 22, wherein the programming ending condition is a pre-selected time.

24. (Original) The apparatus of claim 22, wherein the programming ending condition is an ending address.